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10/693,775	10/25/2003	Ling Chen	AM-5209.D2	1973

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Applied Materials, Inc.
Patent / Legal Dept.
M/S 2061
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EXAMINER	
NGUYEN, TUAN H	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,775	CHEN ET AL.	
	Examiner	Art Unit	
	Tuan H. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-16 and 42-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-16 and 42-67* is/are rejected.

7)☒ Claim(s) *17-41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 12, 17-41, 67 are objected to because of the following informalities:

- Claim 12 is redundant, see claim 8.

- Duplicated claims 17-41 should be canceled.

- Claim 67 depends on cancel claim 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 48-49 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The step of "depositing and removing the first barrier layer within a single chamber" as recited in claims 48-49 are not supported by the instant specification. Note in the instant specification, page 6, bottom paragraph for the step of removing first barrier layer formed by CVD and PVD depositing second layer in the same sputtering

chamber, not depositing and etching the first barrier in the same sputter chamber as claimed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim 63 is rejected under 35 U.S.C. 102(e) as being anticipated by Merchant et al..

See Merchant et al., figs. 1-4 and related text on col. 2-4 which discloses the claimed method for filling one or more of a via and a trench in a pattern substrate including the steps of depositing a generally conformal first barrier layer 12 by CVD (fig. 2, and paragraph bridging col. 2-3); removing the first barrier layer 12 from the

horizontal surfaces of the pattern substrate (figs. 3-4, col. 3, second and third paragraphs); depositing a second barrier layer 14 by PVD (col. 3, fifth paragraph); and depositing one or more conductive material (fig. 4, col. 4, third paragraph).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 64 is rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant et al. in view of Ding et al..

Merchant et al., figs. 1-4 and related text on col. 2-4 which discloses the claimed method for filling one or more of a via and a trench in a pattern substrate as explained above, except the step of depositing a seed layer after the second barrier layer is deposited.

Ding et al., in a related Barrier layer for electroplating processes, as shown in fig. 3, suggests depositing metal seed layer over the barrier layer for a subsequent electroplating process.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have deposited metal seed layer as suggested by Ding et al. in Merchant et al. process since the seed layer would provide good adhesion for a subsequently depositing metal layer (col. 2, lines 47-51).

Claims 42- 47, 50, 52, 53, 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Geffken et al. (cited by applicant) in view of Merchant et al. and Ding et al..

Geffken et al., figs. 1-3E and text on col. 1-3 teaches the claimed method for filling one or more of a via and a trench in a pattern substrate including the steps of depositing a conformal first barrier layer comprises a Ta, TiN, TaN WN, TiSN, TaSiN or silicon nitride as barrier material for forming barrier layer 28; removing the first barrier layer 28 from horizontal surfaces of the patterned substrate (fig. 3C, col. 2, lines 36-48, col. 3, third paragraph); depositing a second barrier layer 29 of Ta, TaN, TiN, WN, WSiN, or TaSiN on the bottom of the trench (col. 3, lines 34-39); and then depositing one or more conductive materials 30 of copper (fig. 3D and text on col. 3, fourth paragraph).

Geffken et al. fail to disclose the use of CVD and PVD for forming first and second barrier layers respectively, and seed layer for a subsequent of electroplating copper.

Merchant et al., in a related art as shown in figs. 1-4 and text on col. 2-3 teaches the use of CVD method for forming the first barrier layer 12 (col. 2, last paragraph), and PVD method for forming second barrier layer 14 (col. 3, fifth paragraph).

Ding et al., in a related Barrier layer for electroplating processes, as shown in fig. 3, suggests depositing copper seed layer by PVD over the barrier layer for a subsequent electroplating process (col. 8, lines 15-65). Note also on col. 2, third

paragraph for suggesting of the use of combination of CVD/PVD to deposit barrier layer 34.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used CVD and PVD for forming first and second barrier layers respectively as suggested by Merchant et al. and Ding et al. in Geffken et al. process for forming barrier layers since CVD and PVD are well-known processes for providing a conformal coverage, improving texture, film properties, and better adhesion.

It would have been also obvious to one having ordinary skill in the art at the time the invention was made to have deposited metal seed layer as suggested by Ding et al. in Geffken et al. and Merchant et al. process since the seed layer would provide good adhesion for a subsequently depositing metal layer.

Claims 48, 49, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Geffken et al. in view of Merchant et al. and Simon et al. (both cited by applicant).

The combination of Geffken et al. and Merchant et al. teaches substantially the claimed method for filling one or more of a via and a trench in a pattern substrate including the steps of CVD depositing a conformal first barrier layer comprises a Ta, TiN, TaN WN, TiSN, TaSiN or silicon nitride as barrier material for forming barrier layer 28; removing the first barrier layer 28 from horizontal surfaces of the patterned substrate; PVD depositing a second barrier layer 29 of Ta, TaN, TiN, WN, WSiN, or TaSiN on the bottom of the trench; and then depositing one or more conductive materials 30 of copper as explained above, except the step of etching and depositing

the first barrier layer in a single chamber, and filling the contact hole with metal by CVD process.

Simon et al., in a bottomless liner structure as shown in figs. 1-4 and col. 3-6, teaches the use of PVD method for sputtered depositing and etching barrier layer in a single chamber (fig. 3, col. 4, last paragraph).

Simon et al. on col. 1, lines 60-62 discloses the well-known techniques for depositing metal layer by either PVD, CVD, electroless deposition or electroplating.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have etched and depositing barrier layer in the same chamber as suggested by Simon et al. in Geffken et al. and Merchant et al. process for simplifying process steps, reducing contamination.

It would have been also obvious to replaced electroplating process with CVD for depositing metal in to the hole since they are well-known processes and the substitution of art recognized equivalent are within level of those skill in the art.

Claims 1-2, 4-16, 42-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et al. in view of Simon et al. (cited by applicant) and Satta et al. (cited ref.).

Ding et al., figs. 1-4 and text on col. 1-9 discloses substantially the claimed method for forming a copper interconnect in a substrate including the step of CVD depositing a first barrier layer, PVD depositing a second barrier layer over the first barrier layer (col. 4, fourth paragraph); PVD depositing a seed layer over the second

barrier layer; and electroplating copper into the hole over the copper seed layer (col. 4, fifth paragraph).

Ding et al. lacks anticipation of forming the first barrier layer by ALD, and etching the first barrier at bottom of the hole.

Satta et al., in a related art as shown in figs. 1-3 and text on col. 4-14 teaches the use of ALD for forming first barrier layer 26 (fig. 2, col. 13, fourth and fifth paragraphs). Note on lines 50-53 for the well-known alternating methods of depositing metal layer such as CVD, PVD, ALD.

Simon et al., figs. 1-4 and col. 3-6, teaches the use of PVD method for sputtered depositing a second barrier layer and etching the first barrier layer in a single sputter chamber by energetic ions (fig. 3, col. 4, last paragraph).

Simon et al. on col. 1, lines 60-62 discloses the well-known techniques for depositing metal layer by either PVD, CVD, electroless deposition or electroplating

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the teachings from Satta et al. and Simon et al. in Ding et al. process for forming and etching the barrier bottom layer since ALD would result in highly conformal layer, and removing the bottom portion of barrier layer would reduce contact resistance (Simon et al., col. 1, lines 47-59), and etching the first barrier layer while depositing the second barrier layer in the same sputter chamber would simplifying the process steps, time and cost as well as reducing contamination by not moving the substrate out of the chamber between the steps.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is 571-272-1694. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan H. Nguyen
Primary Examiner
Art Unit 2813